



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,267	01/02/2004	Peter J. Zdebel	ONS00535	1730

7590 01/10/2006

Mr. Jerry Chruma
Semiconductor Components Industries, L.L.C.
Patent Administration Dept - MD/A700
P.O. Box 62890
Phoenix, AZ 85082-2890

EXAMINER

SOWARD, IDA M

ART UNIT	PAPER NUMBER
----------	--------------

2822

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EF

Office Action Summary	Application No. 10/750,267	Applicant(s) ZDEBEL ET AL.	
	Examiner Ida M. Soward	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 October 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-31 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 20-31 is/are allowed.
- 6) ☒ Claim(s) 1,5-10 and 15-17 is/are rejected.
- 7) ☒ Claim(s) 3-4,11-14,18 and 19 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to the Applicants amendment filed October 31, 2005.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 5-10 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (5,545,909) and Williams (6,060,752) in view of Daly et al. (6,236,087 B1).

In regard to claim 1, Williams et al. teach a semiconductor ESD structure comprising: a semiconductor substrate 1442 of a first conductivity type having a first region 1444 of a second conductivity type and a first dopant concentration; a buried region 1416 of the second conductivity type formed in the first region 1444; a second region 1400 of the first conductivity type formed in the first region 1444; a third region 1408 of the first conductivity type formed in the first region 1444; a first isolation region 1418-center formed in the first region 1444 between the second 1400 and third 1408 regions; a first pair 1402 of oppositely doped regions formed in the second region 1400;

Art Unit: 2822

and a second pair 1410 of oppositely doped regions formed in the third region 1408 (Figure 14, columns 8-10, lines 58-67, 1-67 and 1-10, respectively).

However, Williams et al. fail to teach the second and third regions contacting the buried layer; and the second and third regions and first isolation region from concentric rings in the first region.

Williams teaches second 904 and third 910 regions contacting buried layers 926 & 928 (Figure 9A, columns 6-7, lines 53-67 and 1-18, respectively).

Daly et al. teach the second and third regions 92 & 94 and first isolation region 100 from concentric rings in the first region (Figures 9 and 11, columns 10 and 13, lines 48-67 and 9-33, respectively).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor ESD structure as taught by Williams et al. with the semiconductor ESD structure having second and third regions contacting the buried layers as taught by Williams and the semiconductor ESD structure having the second and third regions and first isolation region from concentric rings in the first region as taught by Daly et al. to protect integrated circuits from electrical overstress and in particular electrostatic discharge (column 1, lines 6-10).

In regard to claim 5, Williams et al. teach the first isolation region 1418-center extending through the first region 1444 and contacting the buried region 1416 (Figure 14, columns 8-10, lines 58-67, 1-67 and 1-10, respectively).

In regard to claim 6, Williams et al. teach the first region 1444 comprising an epitaxial layer (Figure 14, columns 8-10, lines 58-67, 1-67 and 1-10, respectively).

In regard to claim 7, Williams et al. teach the first pair 1402 of oppositely doped regions being shorted together (Figure 14, columns 8-10, lines 58-67, 1-67 and 1-10, respectively).

In regard to claim 8, Williams et al. teach the second pair 1410 of oppositely doped regions being shorted together (Figure 14, columns 8-10, lines 58-67, 1-67 and 1-10, respectively).

In regard to claim 9, Williams et al. teach a second isolation region 1418-left formed in the first region 1444 adjacent the second region 1400; and a third isolation region 1418-right formed in the first region 1444 adjacent the third region 1408 (Figure 14, columns 8-10, lines 58-67, 1-67 and 1-10, respectively).

In regard to claim 10, Williams et al. teach the second 1418-third and third 1418-right regions extending to the buried layer 1416 (Figure 14, columns 8-10, lines 58-67, 1-67 and 1-10, respectively).

In regard to claim 15, Williams et al. teach the buried region 1416 and the second region 1400 form a buried avalanche region (Figure 14, column 12, lines 13-25).

In regard to claim 16, Williams et al. teach the buried region 1416 and the third region 1408 form a buried avalanche region (Figure 14, column 12, lines 13-25).

In regard to claim 17, Williams et al. teach one of the first pair 1402 of oppositely doped regions and the second pair 1410 of oppositely doped regions being shorted together (Figure 14, columns 8-10, lines 58-67, 1-67 and 1-10, respectively). And in regard to the fact one of the first pair and second pair are shorted together, claims directed to apparatus must be distinguished from the prior art in terms of structure

Art Unit: 2822

rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

Allowable Subject Matter

Claims 20-31 are allowed.

Claims 2-4, 11-14 and 18-19 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1, 5-10 and 15-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to semiconductor ESD structures:

Beigel et al. (5,594,266)

Kouno et al. (US 6,365,932 B1)

Lauvray et al. (6,040,604)

Matsunaga et al. (5,212,398)

Art Unit: 2822

Oh (5,986,863)

Rizvi et al. (5,801,065).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
January 8, 2006

Ida M. Soward
AU 2822